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Synthesised signal generator for 10 to 1800MHz

The construction of a high quality signal generator presents a developer with one challenge after another. Several concepts and the most varied approaches to solutions are presented in this article To keep the amount of assembly and wiring as low as possible, and obtain the best possible signal quality, the author developed his own concept which is described below.

1. Introduction

A synthesised signal generator can be used as the signal source for a multitude of measurement and calibration operations. The essential factors in its usability are the range of performance and signal quality.

If we set ourselves the task of constructing a SUPER signal generator to laboratory standards of quality, it soon becomes clear that developing such a piece of apparatus would require a considerable amount of time, and furthermore the cost of realising it should not be underestimated.

So a concept was sought for the development of this signal generator that would keep the amount of assembly work as low as possible but would nevertheless supply a good signal quality, with harmonic signals as low as possible. This led to the "Syn-1800" synthesizer, a solution which has a few interesting details and the following performance:

- Frequency range: 10MHz - 1800MHz in one continuous band
- Smallest frequency division: 1Hz
- Precision of frequency dependent on TCXO/OCXO used
- Output: 0dBm to +10dBm (+13dBm to approximately 1500MHz)
- Power adjustment: in 0.1dB steps Analogue and digital power regulation (only approximately 0.2dB frequency dependence)
- Fully automatic power calibration (digital levelling)
- Digital frequency fine trimming

Technical data for prototype:

- Spectrum purity: (measured at +7dBm output)
- Harmonic attenuation 15 -1800MHz : >= 40dB

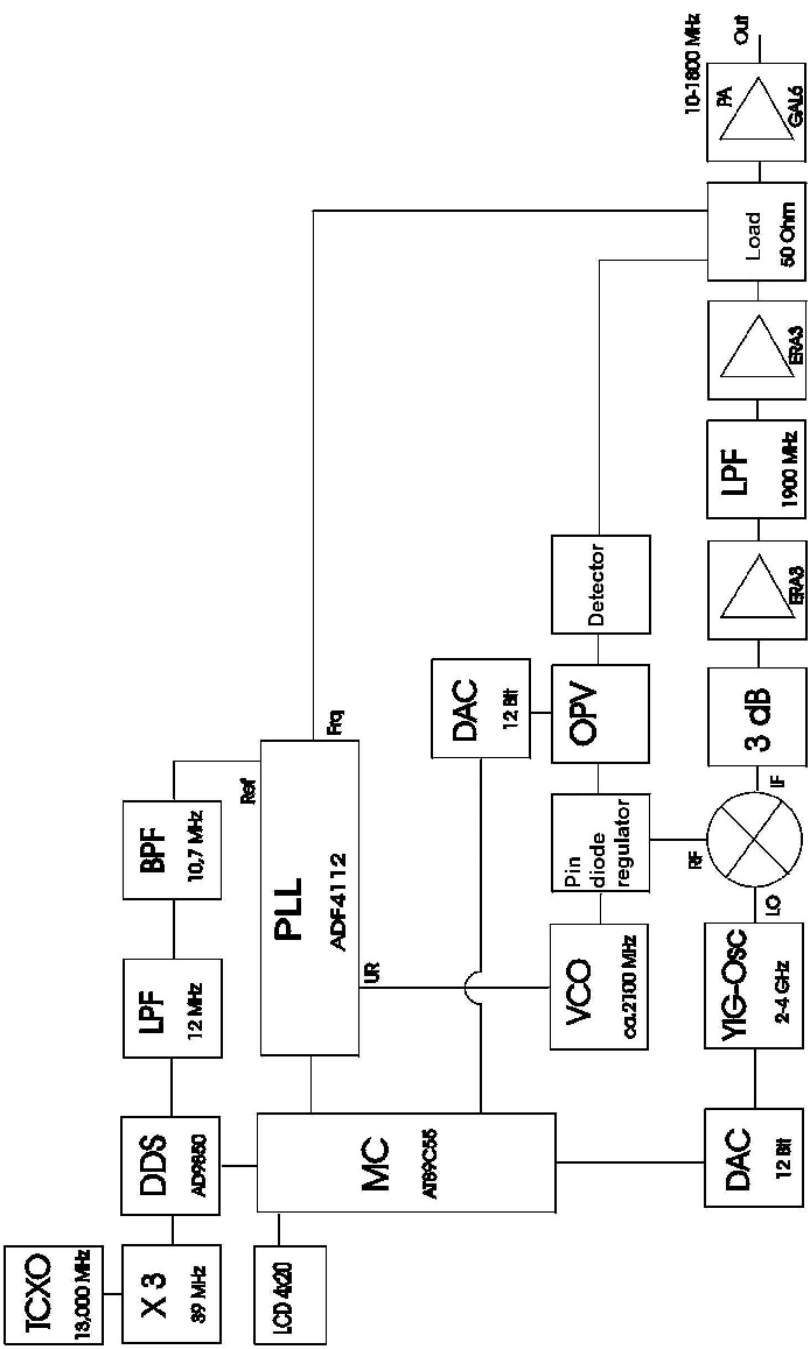

Fig 1: Block diagram of the 10 - 1800MHz synthesised signal generator.

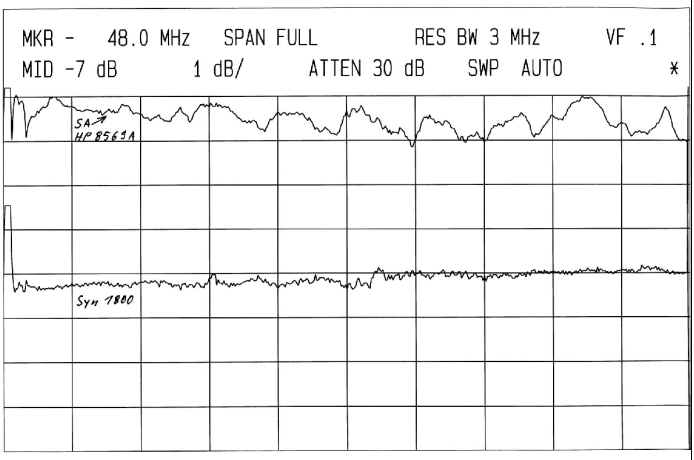

Fig 2: Graph of power regulation from 10 to 1800MHz.

- Harmonic attenuation at 10MHz : 34dB
- Spurious attenuation 10 -175 MHz: >= 40dB
- Spurious attenuation at 1800 MHz: 37dB
- LO suppression (2170MHz): 50dB Image frequency suppression (2180 - 3970MHz): 34dB - 53dB
- Precision of frequency (with 1ppm TCXO used) At 100MHz and 25°C Room temperature: after 10 min time running warm -10Hz: after 20 minutes -6Hz: after 30 minutes - 3Hz

2. Operating principle

The block diagram (Fig 1) provides a view of the individual functional units. The actual frequency synthesiser consists of a YIG oscillator (2 - 4GHz) and a VCO, which runs at approximately 2170MHz and has a tuning range of only approximately 30MHz. The YIG oscillator is tuned by a 12 bit digital to analogue converter.

Both signals are fed into a ring mixer, enhanced and filtered with a steep low pass filter. A small part of the signal generated is fed to the PLL. Only the VCO is re-adjusted with this control voltage. The necessary reference frequency of 10.7MHz is generated by a DDS and fed to the PLL. Using the DDS to generate the reference frequency, it becomes possible to set the output signal in 1Hz steps.

2.1. Advantages of this concept

- Expanded frequency range without band switching.
- Good harmonic attenuation without filter on top.
- The frequency precision is determined only by a reference oscillator (TCXO/OCXO).
- Low construction cost.
- Few manual calibration points.
- Small space requirement giving a small housing.

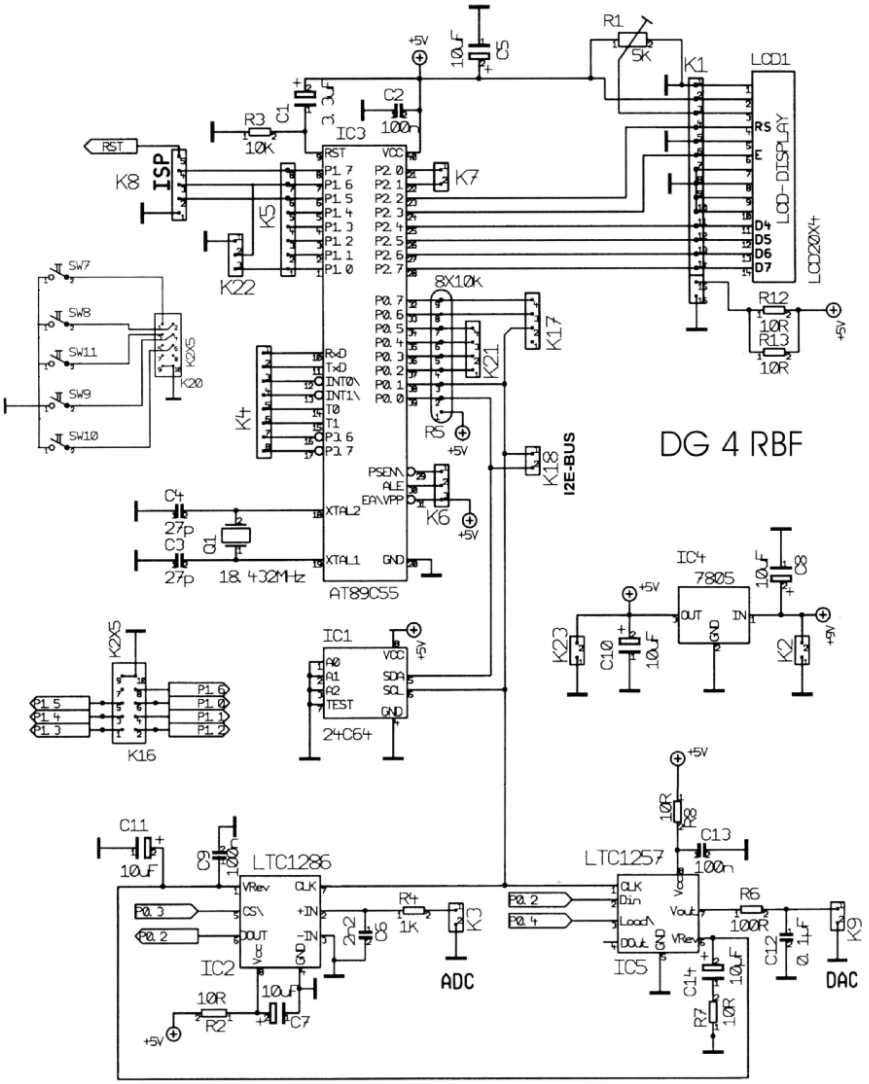

Fig 3 Circuit diagram of the new micro-controller for the 10 - 1800MHz synthesised signal generator.

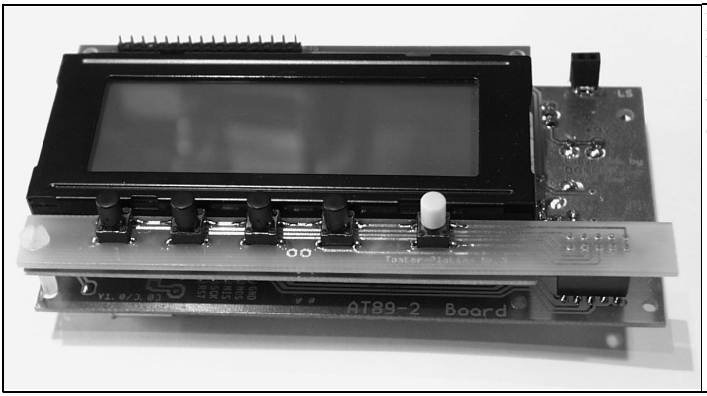

Fig 4: View of the LCD display mounted on top of the micro-controller board.

2.2. Precise power regulation through analogue and digital correction

The signal generator has analogue power regulation, which keeps the level constant, at approximately 1dB, over the entire range. When this is combined with a digital power corrector (corrector values every 10MHz), a very precise power setting is obtained. Thanks to a 50Ohm load at the output, with an additional amplifier for de-coupling, the output level is relatively independent of the load. Fig 2 shows the level regulation in the range from 10MHz to 1800MHz with 1dB/Div. These curves were recorded using an HP 8569A spectrum analyser in MAX HOLD mode, which itself only has a level precision of approximately +/- 1dB (top curve in Fig 2). A wobble generator type EIP 931 was used to give a more precise measurement result by means of the SA's normalising function.

2.3. Cost of implementation

Using this concept and a modular construction procedure, in conjunction with a micro-controller (AT89-2 board), it was possible to keep the cost of implementation comparatively low.

3. The individual components

3.1. AT89-2 microcontroller board

A new circuit (Fig 3) and a new micro-controller board (AT89-2 board) were specially developed for this application, with a 4 line LC display. This equipment can be controlled using push buttons.

The LC display, with 4 x 20 characters, is assembled on one small printed circuit

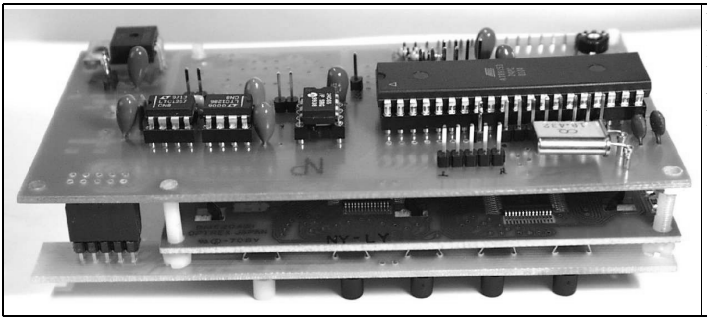

Fig 5: View of the micro-controller board with the LCD display underneath.

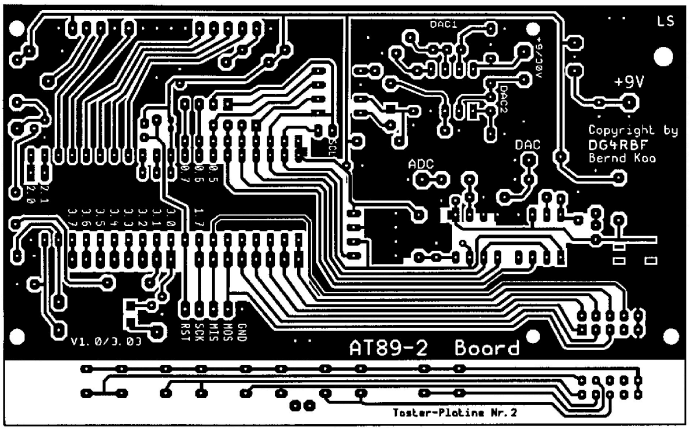

Fig 6: PCB layout for the AT89-2 micro-controller board.

board, and the push buttons are on another. These two boards can be positioned directly on top of the micro-controller board (Figs 4 and 5**).** This dispenses with the expensive wiring for an LCD and buttons and also gives the system more operational security. The micro-controller board can be mounted directly behind the front plate as a complete unit.

The micro-controller board was developed as a single sided board made from 1.5mm thick FR4 material for the AT89C52, AT89C55 and AT89S53 controllers from ATMEL (Fig. 6). These single chip micro-controllers need no EPROM and no external RAM. The program is saved directly in the micro-controller.

The board also has a socket for an EEPROM (24C64), together with the LTC 1286 12 bit AD converter and the LTC 1257 12 bit DA converter, with an internal voltage reference of 2.048V.

Additional components are also provided for on the board for future applications, but the relevant components should not be mounted here.

The single row connector strip attaches the standard 4 x 20 charatcter LCD display (pins 1-14). Pin 15 and pin16 are also accommodated. They can be used

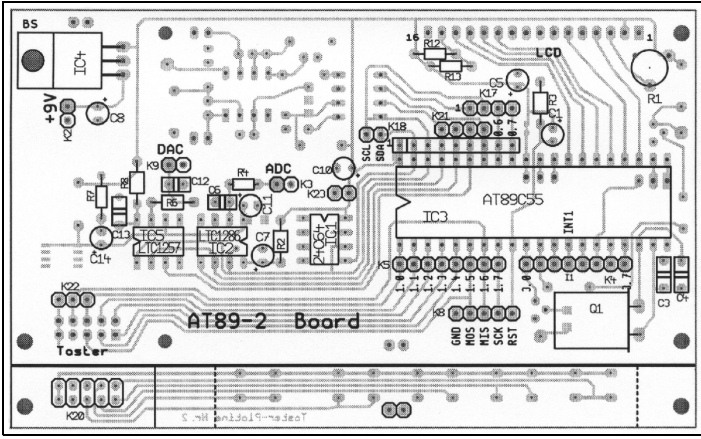

Fig 7: Component layout for the AT89-2 micro-controller board.

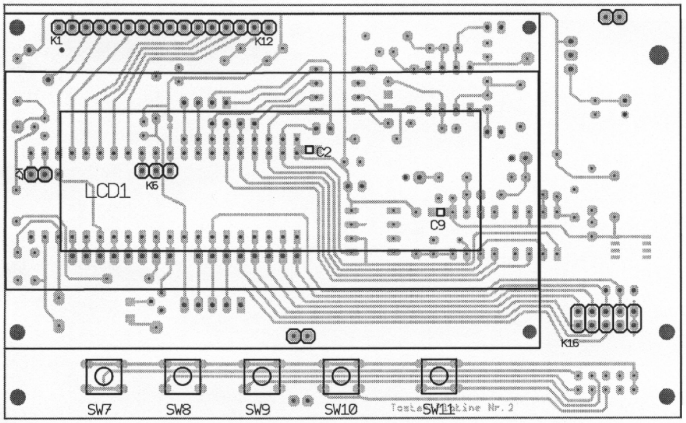

Fig 8: Component layout for the SMD parts on the micro-controller board plus the LCD display and switches

for back lighting. The R1 potentiometer adjust the contrast.

The program for the signal generator is stored directly in the AT89C55 processor. Setup information and calibration data are securely saved in a 24C64 EEPROM and are retained even when the system is switched off.

The narrow button board should be cut off before the components are fitted onto the main board. The components are fitted onto the top and bottom faces in accordance with the component drawings in Figs 7 and 8.

The display board has a 14 pin (16 pin) connector strip and the processor board has a 14 pin (16 pin) socket terminal strip; thus the display can simply be plugged on but remains detachable.

IC sockets should be used for the micro-

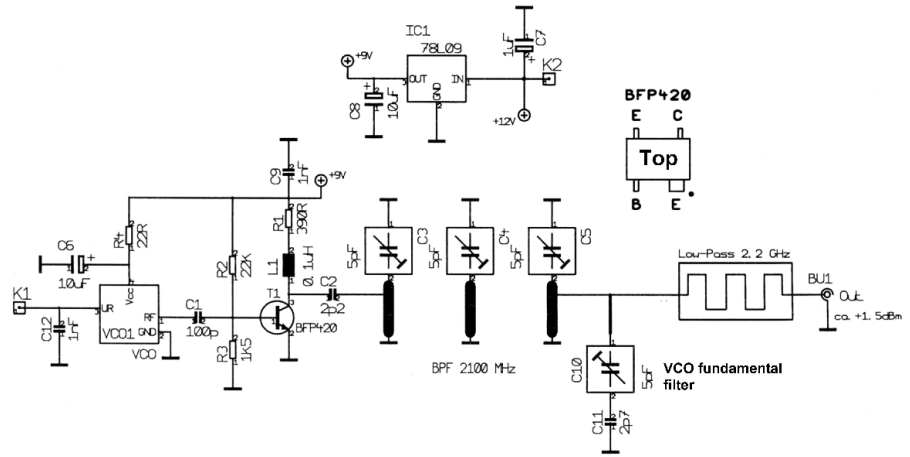

Fig 9: Circuit diagram of the VCO for the 10 - 1800MHz synthesised signal generator.

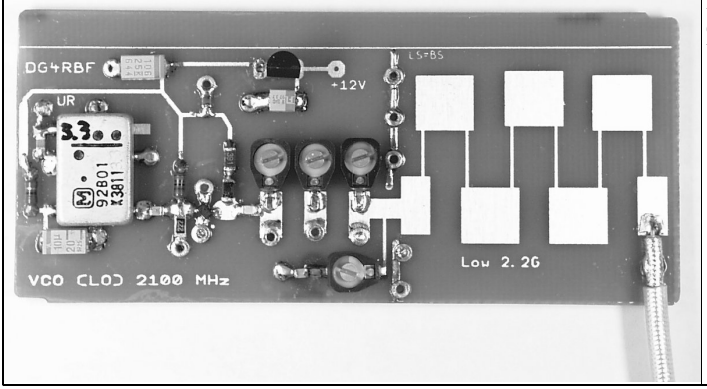

Fig 10: The completed VCO board.

controller and the EEPROM. If desired, the DA and AD converted can be inserted into IC sockets.

3.2. VCO assembly

A narrow band type of VCO is used, which should have a range of approximately 30MHz in the range between 2100MHz and 2200MHz. The search for a suitable VCO for this range turned out to be difficult, but it proved to be considerably easier to obtain VCO's with an output frequency of around 1000MHz. For this reason, a VCO producing approximately 1090MHz was chosen with a doubler stage.
A low pass filter, which would have been needed in any case, was integrated directly onto the 1.5mm thick epoxy printed circuit board (FR4).

3.2.1. VCO Operation

The VCO is followed by a doubler stage, using a BFP 420 from Siemens (Fig. 9).

This is followed by a three stage band pass filter using microstrip circuit technology. There is also a filter circuit for the fundamental frequency of the VCO (1090MHz) that suppresses it by up to 70dB.

It does not make sense to mount this filter circuit (C10 + C11) unless a spectrum analyser is available to calibrate it. Without a filter circuit, the fundamental frequency can still be attenuated up to approximately 45dB, which is still adequate.

At the output there is a 13 pole "printed" low pass filter, which is laid out for a cut-

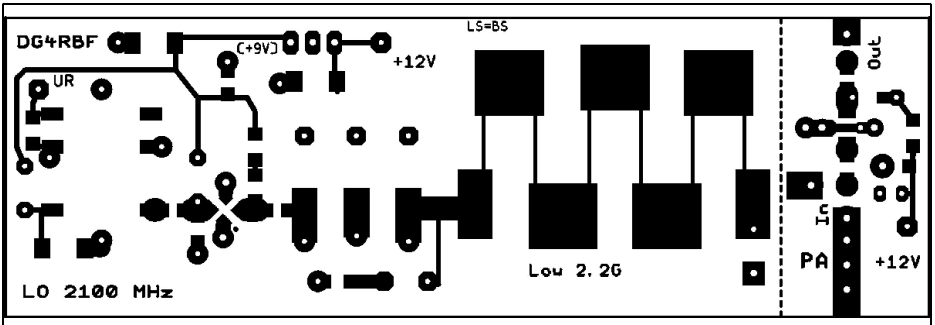

Fig 11: PCB layout of the VCO and PA boards.

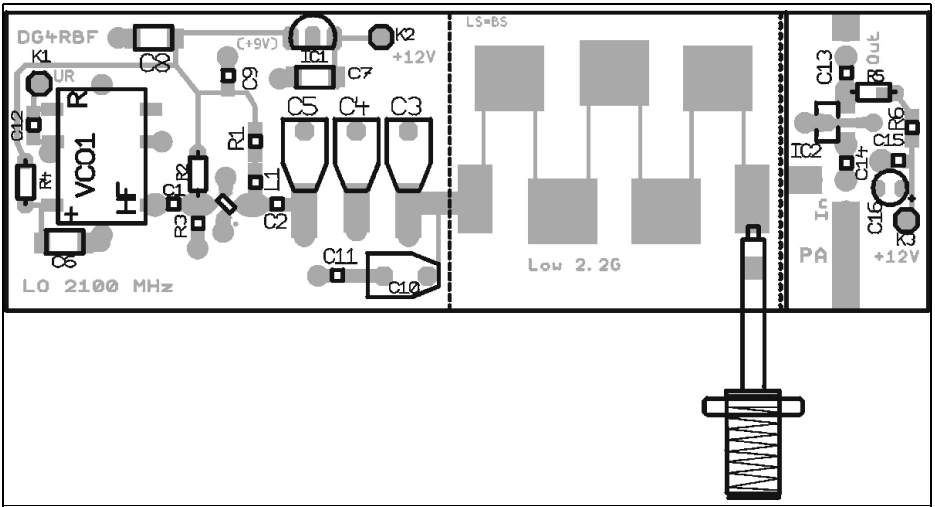

Fig 12: Component layout of the VCO and PA boards.

off frequency of approximately 2200MHz and needs no calibration (Fig. 10).

3.2.2. VCO Assembly instructions

The layout of the 107mm x 35mm VCO board (FR4), is shown in Fig. 11. The components are mounted on the component side in accordance with the component drawing in Fig. 12.

The completed board is fitted into a tinplate housing and well soldered to the earthing side. The board is slightly shorter than the standard housing, but this is not important. In order to avoid a waveguide effect when a lid is placed on top, and to ensure that the higher frequencies can overcome the low pass filter without interruption, either a partition must be soldered on at the marked point following the band pass filter or a piece of conductive foam material must pressed into the upper part of the housing. There are through connections on the board for soldering the partition.

3.2.3. VCO Calibration

If no spectrum analyser is present, then calibration is not possible, except using an mW meter. For this purpose, the trimmer of the band pass filter is turned to the minimum and then set to an overlap of approximately 1mm. The setting is then altered from this basic setting to the maximum value by gently rotating the trimmer with a (non-metallic) trimming tool. When the maximum value has been found by rotating the trimmer in each direction and the capacitor plates of the trimmer overlap only slightly, the calibration is correct. You should expect a signal level of approximately +1.5dBm. You cannot calibrate at the wrong frequency unless you rotate the trimmer too far (approximately halfway); then you'd be calibrating at 1080MHz!

If a spectrum analyser is present, the filter circuit trimmer can be set for minimum output of the fundamental frequency. This cannot be calibrated properly unless the board has been soldered into the tinplate housing. Since the filter circuit has a very narrow bandwidth, a control voltage of approximately 3.8V should be applied to the VCO and the lid's capacity should also be taken into

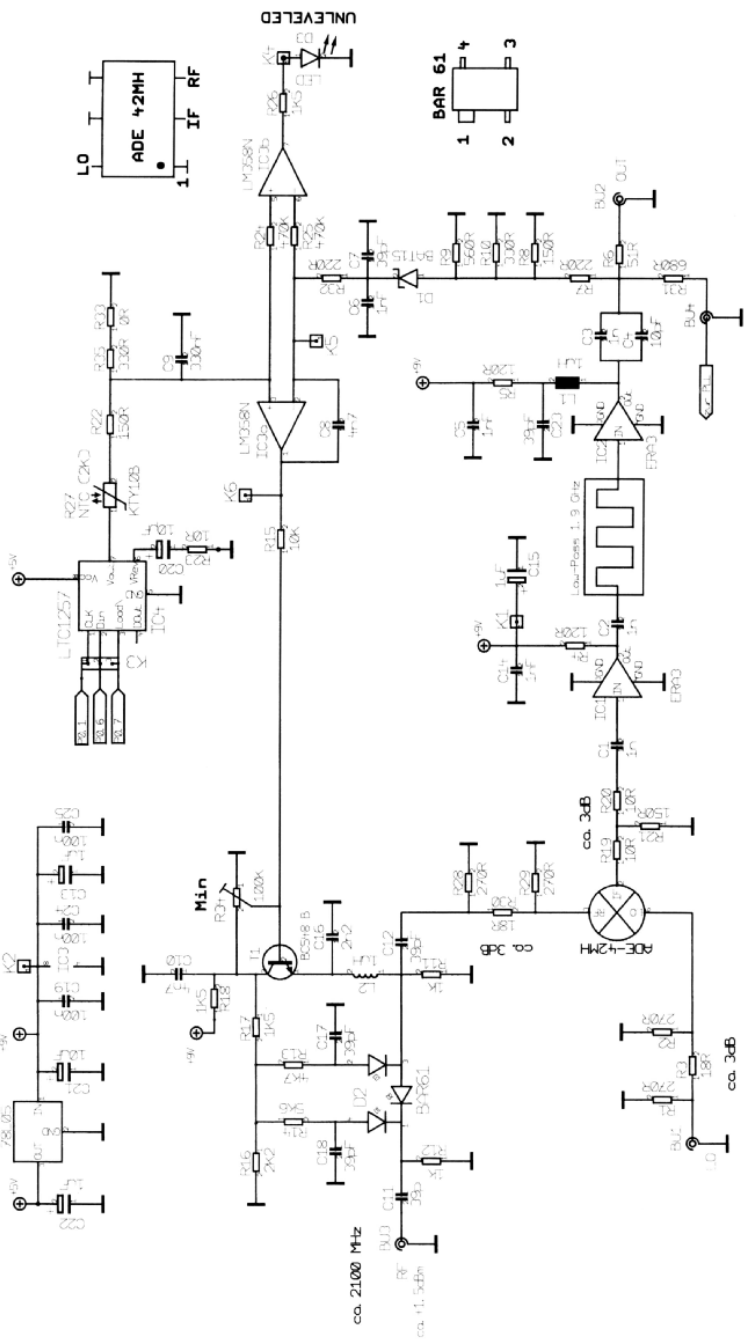

Fig 13: Circuit diagram of the mixer for the 10 - 1800MHz synthesised signal generator.

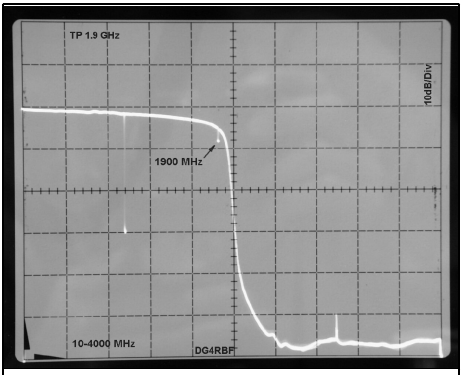

Fig 14: Frequency response of the 21 pole filter at the output of the mixer.

account.

3.3. Mixer assembly operation

The signal from the YIG oscillator is connected to socket BU1 (Fig. 13). Following an attenuator of approximately 3dB, the signal is fed to the ADE 42-MH mixer LO port. Approximately +13dBm should be detectable at the LO port, an acceptable signal is in the range between +10dBm and +15dBm.

The mixer can process frequencies between 5 and 4200MHz at the LO and RF ports, so that the intermediate range extends from 5 to 3500MHz. The signal from the VCO is connected to socket BU3. The level is set by means of the adjustable PIN diode attenuator (PIN diodes), using the BAR61 diode. This is fed to the RF input of the ring mixer via a 3dB attenuator.

A 3dB attenuator is also provided at the (intermediate frequency) mixer output to ensure that good phasing is obtained, and reflections are kept to a minimum. This is followed by two ERA3 MMIC amplifiers and a very steep 21 pole low pass filter with a cut-off frequency of approximately 1900MHz. This filter, which DG4RFB developed himself, takes the form of a microstrip and has already proved itself in various circuits. The steep flank of the filter is very important, since it has to suppress the LO signal at approximately 2190MHz, together with the image frequencies (Fig. 14).

The output is terminated with a 51Ohm resistor, which helps to make precise power regulation possible. For power regulation (levelling), some power is sampled before the 51Ohm resistor (R6), rectified using diode D1 (BAT15) and fed to an OP (IC3a), which re-adjusts the attenuator at the mixer input so that the output is kept constant.

Theoretically, such regulation circuits are extremely simple. In practice, however, it is often difficult, with broad band circuits of this kind, to obtain an “orderly” frequency response. Power levels within approximately 1 dB can be obtained in the frequency range between 10 and 1800MHz using the circuit presented here. Fig 2 shows the level regulation in the frequency range indicated at 1dB/Div. This curve was again plotted using an HP 8569A spectrum analyser, using the EIP 931. The lower curve in the diagram shows the test results.

At first glance, the parallel resistors R9 - R11, before the detector diode D1, seem to have no purpose, but these resistors can be used to influence the frequency response of the regulation circuit. If the resistance value is increased, then the power at the band end is increased, and vice versa. Thus varying these resistors can optimise the frequency response.

Digital power setting is achieved using the LTC 1257 12 bit DA converter (IC4). A defined voltage is applied to pin 3 of the regulation OP. The LTC1257 has an internal voltage reference of precisely 2.048V. At the output of the DA converter there is an NTC, together with a voltage divider. The resistance ratio of the voltage divider scales the output voltage for power regulation. The NTC compensates for the temperature coeffi-

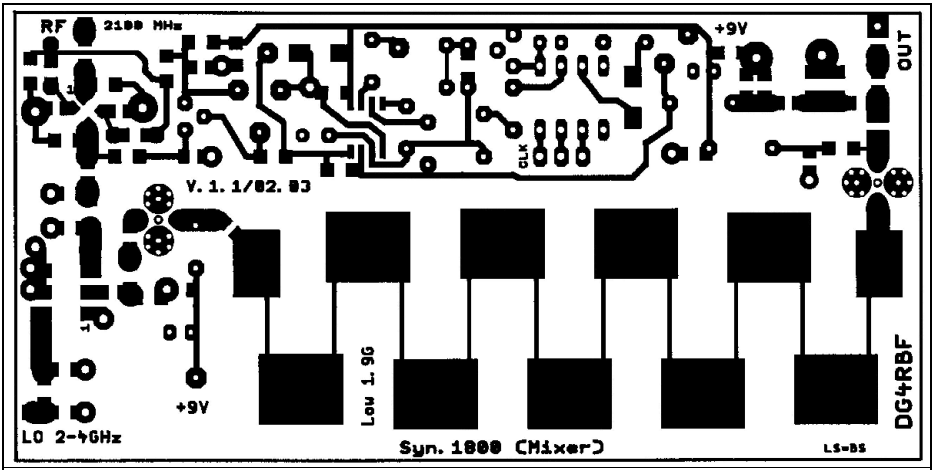

Fig 15: PCB layout for the mixer and filter.

cient of the detector diode (BAT15). It is possible to obtain quite good temperature compensation using the NTC. R33 is not normally required, and is provided only to give more options if another divider ratio is needed on the voltage divider. The second OP (IC3b) detects situations when the required power is not maintained and lights the UNLEVELED diode.

3.3.1. Mixer assembly instructions

The 109mm x 54mm printed circuit board layout for the mixer board is shown in Fig 15. All components are mounted on the foil side of the board (Fig 16). An IC socket is used for the LTC1257 DA converter. Make sure C12 is precisely positioned. When the components have been mounted, the board can be soldered into the tinplate housing. The

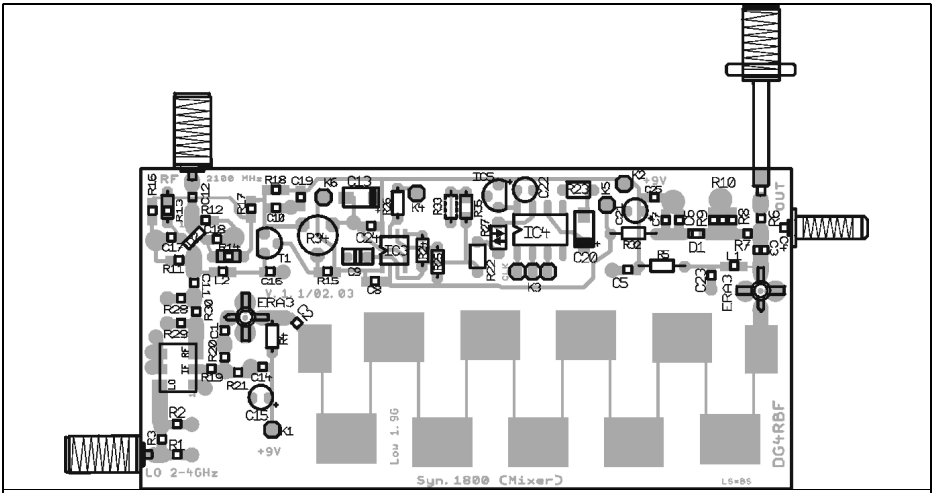

Fig 16: Component layout of the mixer.

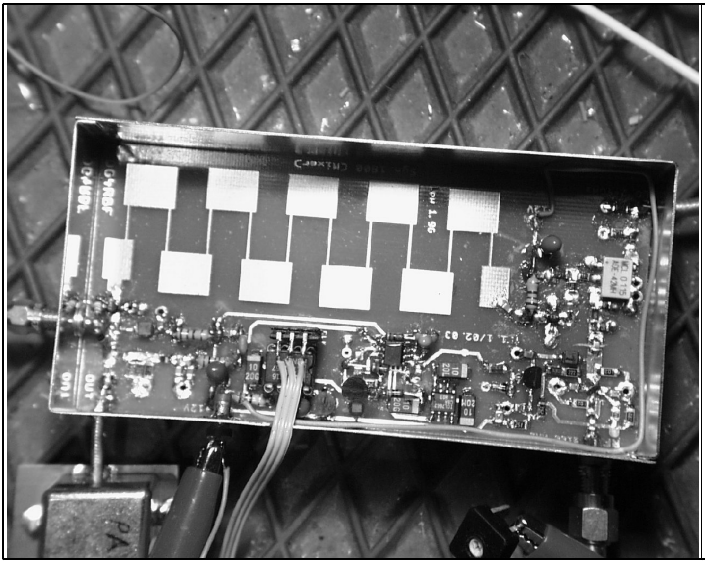

Fig 17: Picture of the completed mixer assembly.

power lead uses of a feedthrough capacitor. It is best to use SMA sockets for the RF inputs. The output is a flexible RF cable feeding the GAL6 PA.

The circuit diagram shows R31, which feeds some power to the PLL. This resistor is not positioned on the board, but is soldered on separately and leads to a nearby SMC socket. Fig 17 shows the completed mixer assembly.

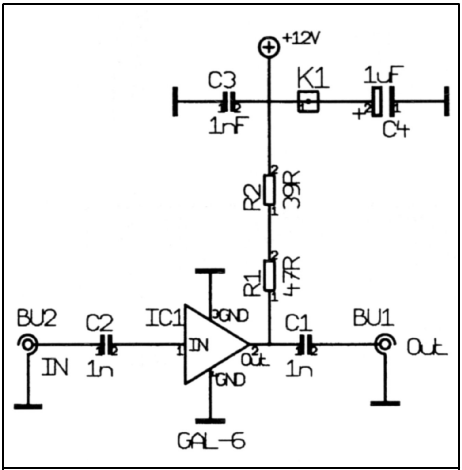

Fig 18: Circuit diagram of the GAL-6 output amplifier.

3.4. Output amplifier with GAL 6

The mixer board is followed by a separate output amplifier, which consists of a GAL 6 type MMIC from Mini Circuits. This component has similar performance to the ERA 6 and a very smooth frequency response, together with a high IP3 of 35.5dBm. It is thus extremely suitable for maintaining a signal with low harmonics.

By using this amplifier after the level regulation, an additional de-coupling from the output is obtained, so that the output regulation acts independently to the load at the output. This means that even if the connected load is mismatched the correct power is generated.

The circuit can be seen in Fig 18. The few components in the "PA" are assembled on a small board (see Fig 11, right) and then soldered into a small housing, or protected using a screening box.

The PA's output should be fitted close to the output socket of the apparatus. To simplify the board manufacture, the small

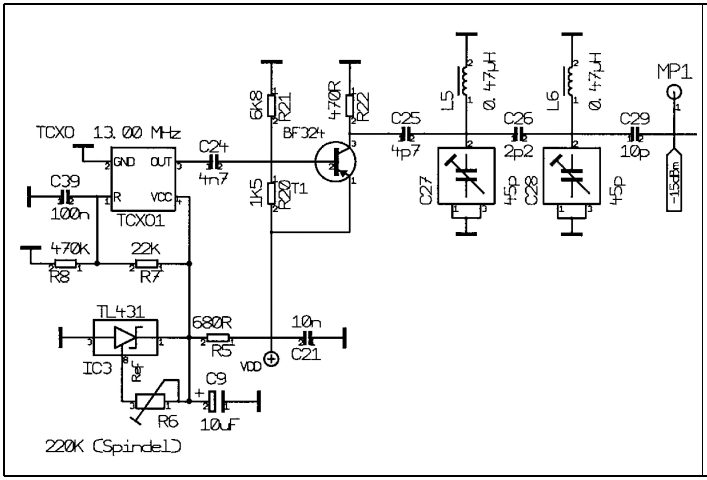

Fig 19: Circuit diagram of TCXO section of the PLL/DDS assembly.

board was added the VCO board, and should be cut off before assembly.

3.5. PLL/DDS assembly

In order to ensure that it can be copied easily, this assembly is divided into three construction sections and the assembly is described here step by step.

3.5.1. PLL/DDS operation

Construction section (1) includes the TCXO, with tuning and frequency tripling. A 13MHz (1ppm) temperature compensated quartz oscillator (TCXO) is used as a frequency reference. An adjustable voltage reference (TL431) of approximately 2.5 V is used for the power supply and tuning voltage. The fine setting can be adjusted to precisely 13MHz using the spindle trimmer. The TCXO is followed by a BF324 frequency multiplier and a 39MHz band pass filter (Fig 19).

Construction section (2) concerns the DDS, with filter and amplifier stage. The DDS generates the reference frequency of the PLL and generates a 10.7MHz signal, which can be tuned in very small steps, from the clock frequency of 39MHz. The familiar AD9850 from Analog Devices is used as the DDS.

At the output of the DDS is a low pass filter with a cut-off frequency of approximately 12MHz. This signal is then amplified by an MSA886 and filtered by a matched 10.7MHz ceramic filter (Fig 20).

The PLL is contained in construction section (3). The ADF4112 is used, a modern component from Analog Devices. This PLL operates at up to 3GHz, has very good noise values and is used here with a pre-divider factor of only 8/9. The PLL component is programmed through a 3 wire bus by the microcontroller. Anyone interested in finding out more about this PLL component should consult the 24 page data sheet from Analog Devices. One important element in the PLL is the loop filter, which can be found at pin 2. Low loss foil capacitors should be used for the loop filter capacitors if possible. Since the PLL has to operate over a very wide range, the loop filter is naturally never optimally designed. Fortunately, the current for the charge pump can be programmed in 8 stages (0.63mA - 5.0mA), so that a certain matching can thus be achieved to the wide frequency range. An additional problem that has to be overcome is that the PLL does not normally

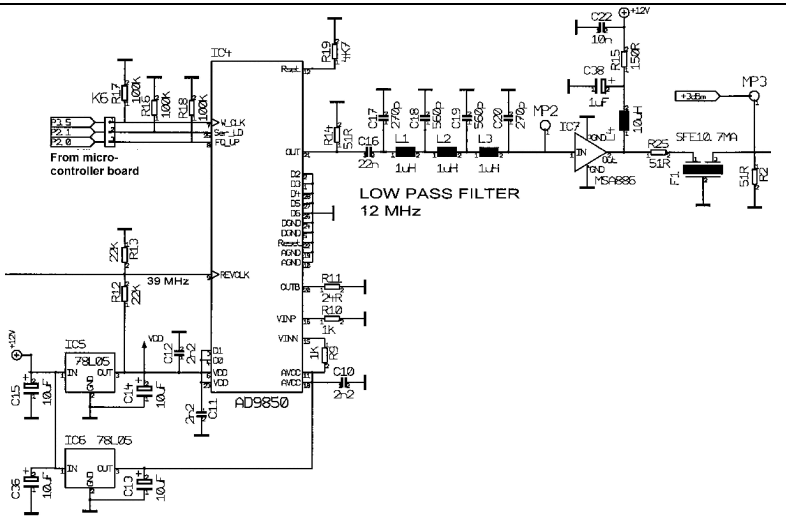

Fig 20: Circuit diagram of the DDS section of the PLL/DDS assembly.

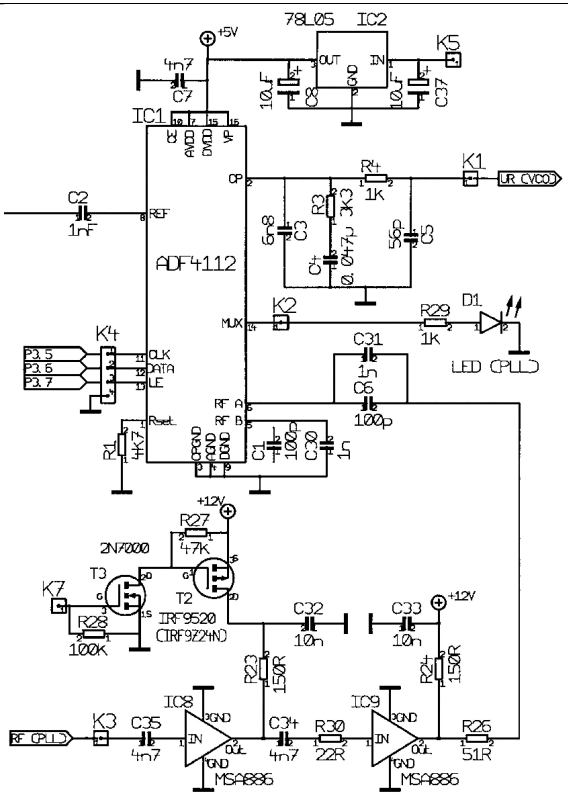

Fig 21: Circuit diagram of the PLL section of the PLL/DDS assembly.

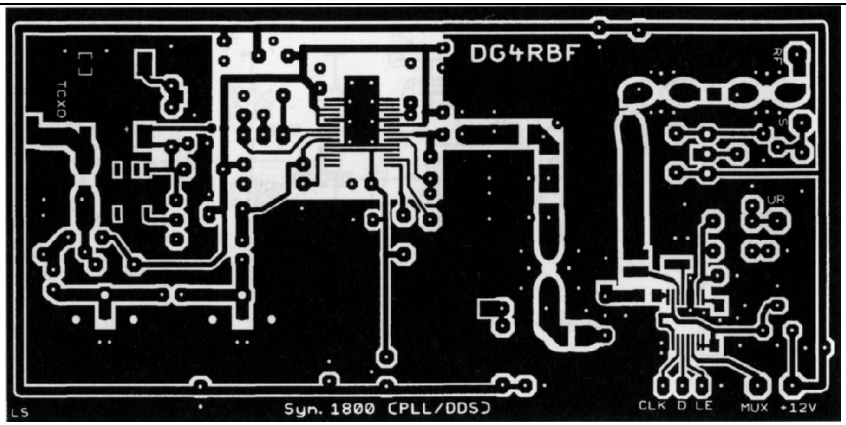

Fig 22: Track side PCB layout for the PLL/DDS board.

function below 100MHz. Below 100MHz a square wave signal can be used for the drive. Here we simply used an additional amplifier (MSA886), which is connected via the two transistors T2 and T3. If the power supply for this MMIC is switched off, then it works as attenuation. If it is connected up, then the subsequent amplifier IC9 is saturated and the PLL operates down to under 10MHz. The "MUX" output of the PLL is programmed as "Lock Detector" switching the LED on if the PLL is locked (Fig 21).

3.5.2. PLL/DDS assembly

Figs 22 and 23 show the PCB layout of the PLL/DDS board and Figs 24 and 25 show the component layout.

Construction section (1)

1 Through hole plate printed circuit board and fit into tinplate housing, but do not solder it in yet.

2 The pin holes, that are not used as earths. must be cleared on the "earthing side". (Sections 1 and 2

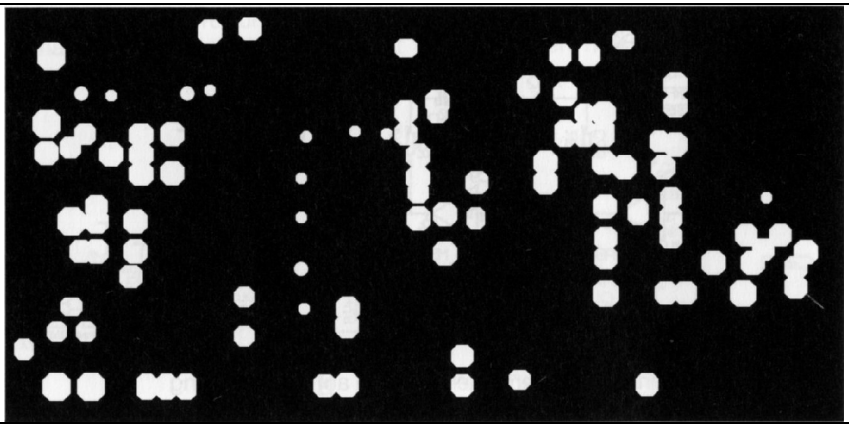

Fig 23: Component side PCB layout for the PLL/DDS board.

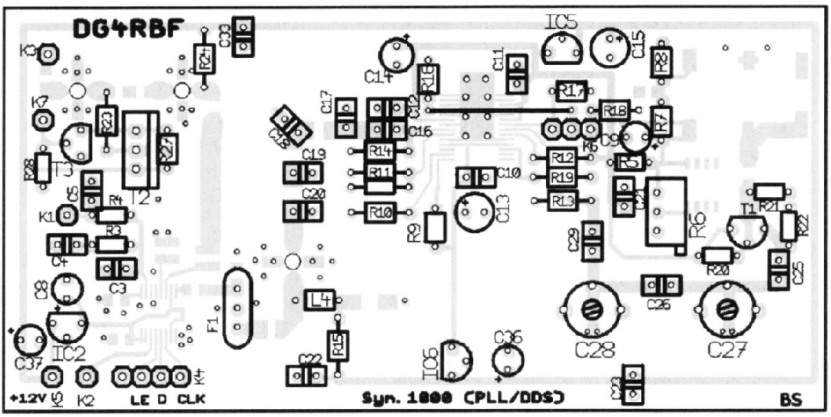

Fig 24: Component layout for the PLL/DDS board.

are not needed unless you are making the board yourself)

3 Fit the 3 regulators (78L05) with the associated filter electrolytic capacitors. Then connect up the 12V power supply and check that the voltage is 5V.

4 Fit all components for this section (1).

5 Turn trimmers C27 and C28 to maximum capacity.

6 Connect an mW meter to (MP1).

7 In turn, tune each trimmer slowly backwards, set them for the maximum level. Then set the trimmer to approximately half.

8 Use a frequency counter to check for 39MHz at (MP1).

Construction section (2)

1 Mount all the components for this section. Before the DDS IC is soldered in, the soldering pads are tin-plated on the board. The IC can then be soldered on, using a small

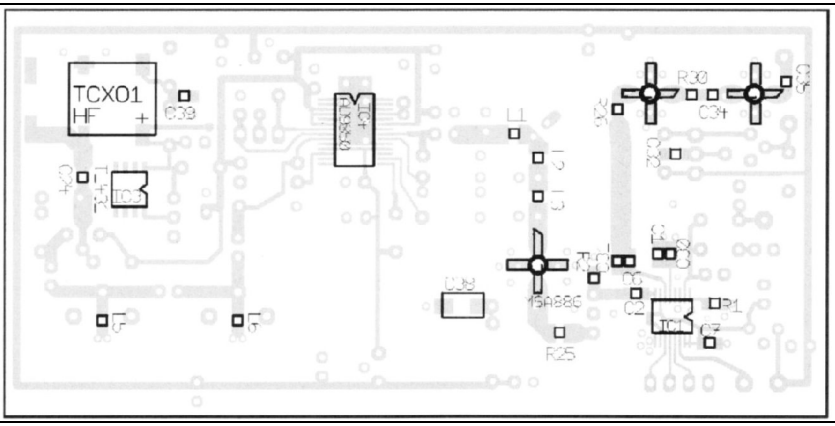

Fig 25: SMD component layout for the PLL/DDS board.

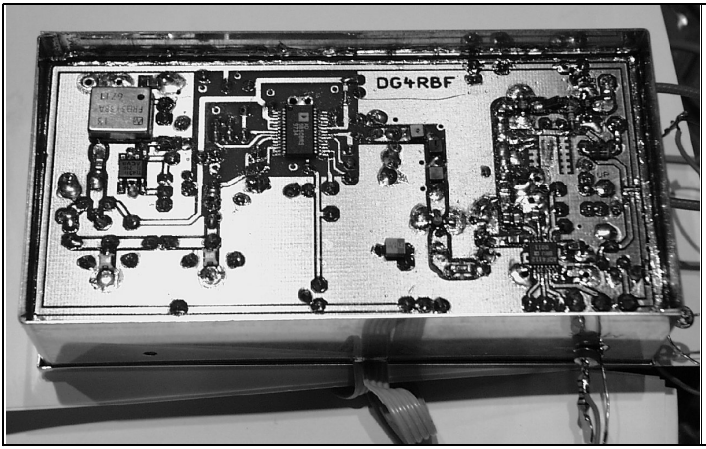

Fig 26: Completed PLL/DDS unit.

SMD soldering iron, without adding any more solder. The solder on the board should suffice. It is helpful to use a magnifying glass when soldering on this IC. But at any rate the soldering must be inspected using a magnifying glass. Don't forget solder bridges at K6.

2 To check the functioning of this construction section, the micro-controller must be connected to K6. Once it has been switched on, the DDS IC is provided with the required data and a 10.7MHz signal should be available on (MP3) at approximately. +3dBm.

3 If a spectrum analyser is available, then this signal should be set with C27+C28 at the lowest noise level. (But this is not absolutely necessary.)

Construction section (3)

1 Mount all the components for this section. The PLL IC can be soldered in using the same technique as in construction section 2. When connecting up the LED D1 at K2, don't forget the resistor.

2 The PLL cannot be tested until all assemblies have been wired together.

Figs 26 show the PLL/DDS assembly

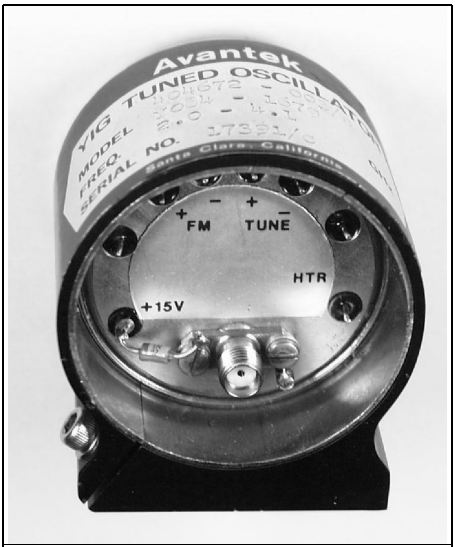

Fig 27: YIG oscillator used in the prototype.

3.6. YIG oscillator

A YIG oscillator with a frequency of 2 - 4GHz is used as the main oscillator. These oscillators have recently become available on the surplus market at reasonable prices. Fig 27 shows the YIG used from Avantek.

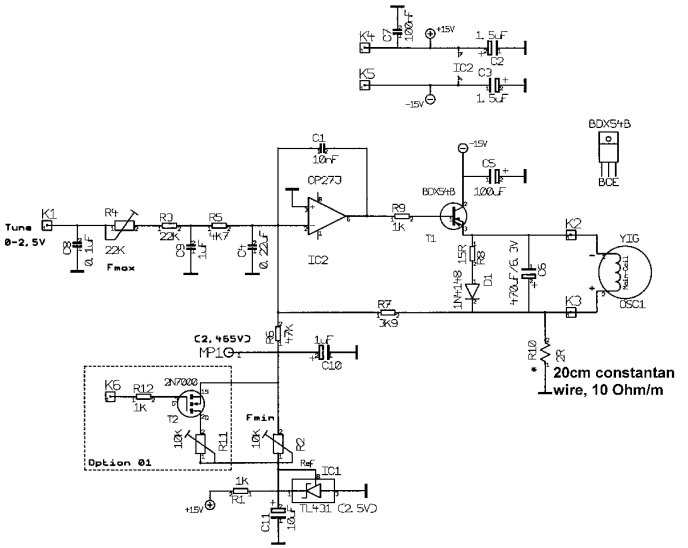

Fig 28: Circuit diagram of the YIG driver.

3.7. YIG driver

A YIG oscillator has at least two tuning coils, the main coil which is designated as "TUNE" and is used for tuning over the entire range and the FM coil for fine tuning or FM modulation. The frequency of the YIG oscillator is proportional to the current that flows through the tuning coil. Thus a YIG driver is also needed to drive the oscillator. The circuit variant used has a setting for the tuning gradient (Fmax), plus the addition of an offset value (Fmin), Fig 28. The oscillator can thus be best matched to the tuning conditions. A reverse coupling through R7 serves to make sure that the frequency remains stable when the oscillator warms up. An important factor here is the resistor R10, which consists of 20cm of constantan wire (10 Ohm/m) and which is made into a small air-core coil. This circuit has proved itself extremely well in practice. The BDX 54B power transistor must be mounted on a heat sink. Fig 31 shows this board. The micro-controller

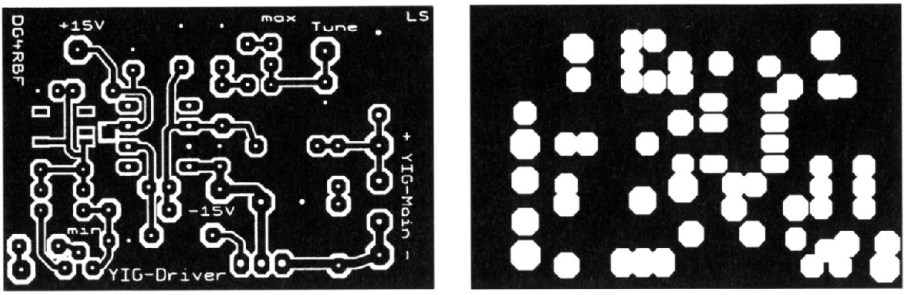

Fig 29: PCB layout for the YIG driver.

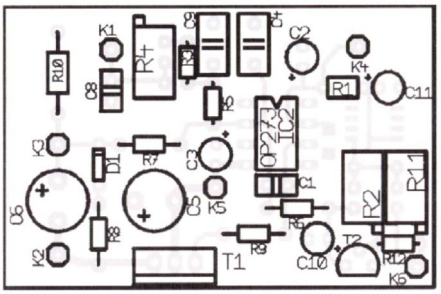

Fig 30: Component layout fro the YIG driver

must be connected to the YIG driver using a screened cable. The option 01 which is specified on the wiring diagram and the components drawing is not fitted. Figs 29 and 30 show the PCB layout for the YIG driver and Fig 31 shows the completed assembly.

3.8. RF ON/OFF

The 12V supply voltage of the VCO and the YIG oscillator is connected so that the RF output of the signal generator can be switched on and off. Two FET's are used for this purpose, see Fig 32 which shows the small circuit.

3.9. DC amplifier for automatic calibration

The signal generator has an automatic calibration function, which makes it possible for it to keep the output very constant over the entire frequency range.

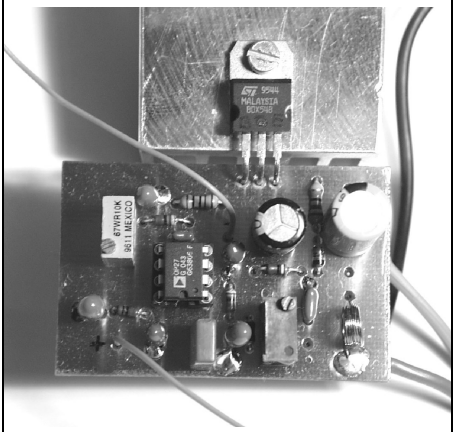

Fig 31: The completed YIG driver assembly.

For this purpose, a diode detector with a frequency response as good as possible must be connected to the AD converter (LTC1286). This 12 bit AD converter is completely matched at an input voltage of +2.048V. But since a diode detector gives only approximately 1.2V at an input of +13dBm, we still need some further amplification for this DC voltage. Most detectors output a negative voltage. A simple OP connected as a DC voltage amplifier can solve both problems. The OP can be switched to accommodate a detector with negative or positive voltage. The amplification is matched to the detector by means of a potentiometer. Fig 33 shows the circuit. Since this amplifier consists of only a pair of components, the

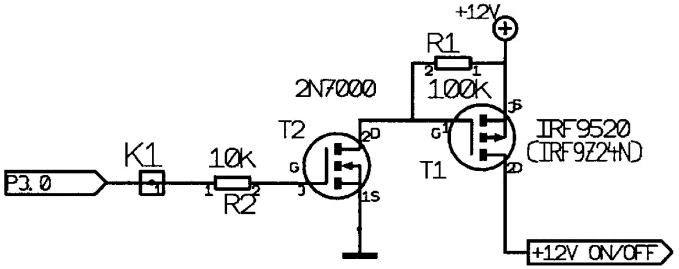

Fig 32: Circuit diagram for the RF On/Off control.

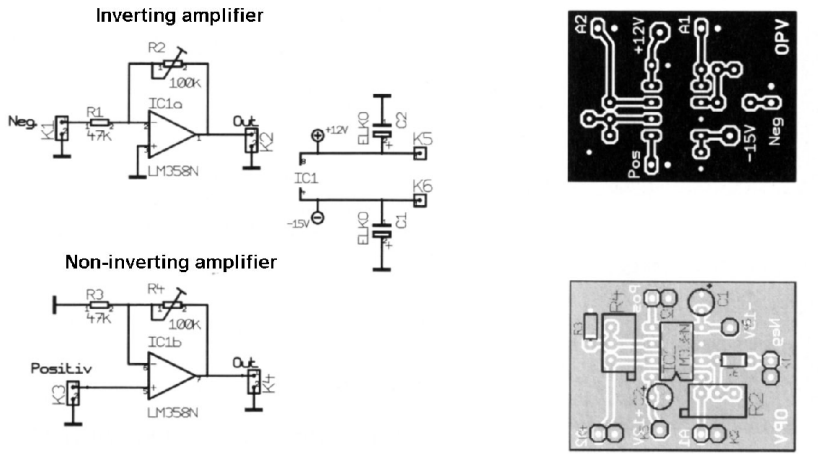

Fig 33: Circuit diagram for the calibration amplifier showing the two alternatives for positive or negative inputs plus a PCB layout.

simplest way to assemble it is on a small breadboard or using the "open air" technology. The input of this amplifier is best fitted on the rear face of the signal generator (BNC socket).

4.

General assembly instructions

For a DIY board, the through platings are manufactured using 1.4mm compression

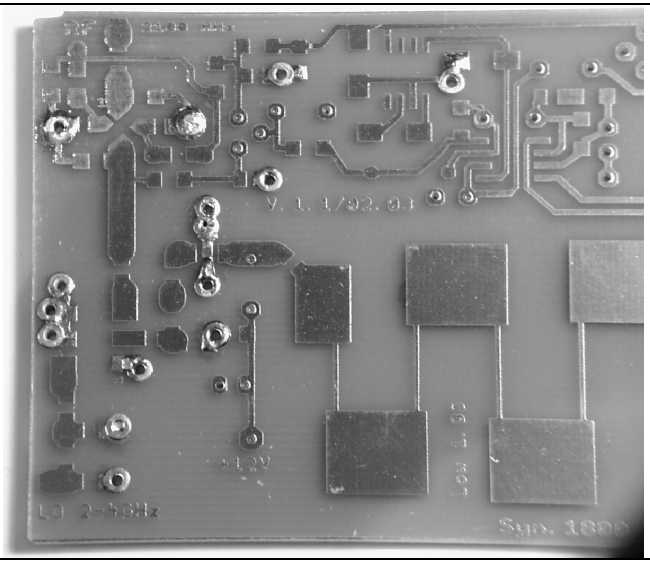

Fig 34: Example of through hole plating.

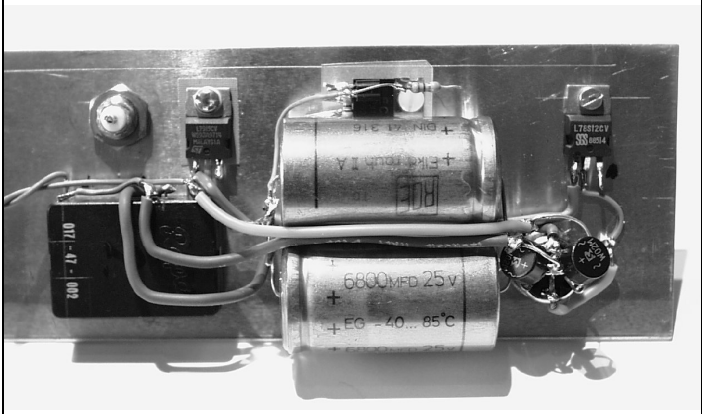

Fig 35: Power supply components mounted on the rear panel of the unit.

rivets (cable sheaths). This also applies to the MMIC's. A large through plating is positioned at each connection to earth of the ERA3. The through platings are already present on industrially manufactured boards.

4.1. Instructions on through plating

For high-frequency circuits it is very important to make sure the connections to earth are good. On a double sided board, the underside (earthing surface) is the only correct earth for high frequency use. If the earth needs to be on the topside of the board, make sure there is a good, low inductance through plating. It is important in this context that the shortest route earths as many "surfaces" as possible. This can be achieved by manufacturing several small through platings or one big through plating. The use of relatively large compression rivets has proved efficacious for DIY etched boards. I use cable sheaths made from copper for this purpose, which are available at reasonable prices for 0.5 / 0.75 square cable. The external diameter is then 1.4 / 1.8mm. The head of the cable sheaths is knocked flat before being soldered into the board. This can be done simply, by generating an appropriate hole in a piece of metal, inserting the cable sheaths into this hole and knocking the head flat with a light blow from a hammer. The cable sheaths prepared in this manner are then pressed into the board and soldered above and below. The ends left over on the bottom side are then ground off or filed off. Fig 34 shows the through platings.

4.2 Incorporation into a housing

If a small housing is used, as for the prototype, then a small fan (CPU fan, as used in computers) should be built into the rear panel. The fan can be set to run slowly and thus gently by means of a suitable series resistor. This ensures uniform temperature conditions and thus stable values for the frequency and the output.

4.3. Power supply

It is very advantageous if the transformer used is not placed in the signal generator housing, since even well screened transformers transfer a 50Hz hum to the circuit. The author uses a transformer with connecting cables which deliver 2 x 12V AC voltage at 1A. The rectification and stabilisation then takes place in the apparatus itself. Fig 35 shows the bridge rectifiers, voltage regulator and filter electrolytic capacitor, which are mounted directly on the rear panel of the housing. For this version of the power supply, a two pole switch must be used.

Table 1: Interconnections between assemblies.

Micro-controller	Mixer Board	Port	Plug	Pin	Function
K17	2	P0.1	K3	1	DAC clk
K17	3	P0.6	K3	2	DAC data
K17	4	P0.7	K3	3	DAC load
Micro-controller	**PLL/DDS board**	**Port**	**Plug**	**Pin**	**Function**
K4	8	P3.7	K4	3	PLL LE
K4	7	P3.6	K4	2	PLL data
K4	6	P3.5	K4	1	PLL clk
K7	1	P2.0	K6	3	DDS soldering pad
K7	2	P2.1	K6	2	DDS data
K4	6	P3.5	K6	1	DDS clk
K4	4	P3.3	K2		MUX/PLL error
K4	5	P3.4	K7		Hi/Lo for PLL
K4	1	P3.0			RF On/Off switch
K5	8	P1.7			RF On/Off button

4.4. Inter-connecting assemblies

Table 1 and Fig 36 show the interconnections and will be of assistance for wiring up the assemblies.

5.

Putting into operation and calibration

The YIG driver must be set first. At this point, the tune voltage, which comes from the DA converter, has not yet been connected to the YIG driver. Nor has the VCO regulator voltage, which comes from the PLL.

The calibration on the YIG driver then proceeds step by step.

1 Connect spectrum analyser or frequency counter to the output.

2 Turn “Fmin” potentiometer all the way to the right.

3 Turn “Fmin” potentiometer all the way to the left, until a reading of approximately 25MHz appears at the output.

4 Set the Syn 1800 signal generator to 10MHz and connect the tune voltage from the DA converter to the YIG driver. The frequency must now increase to approximately 35MHz.

5 Use “Fmin” to select 35MHz.

6 Set Syn 1800 signal generator to 1010MHz and use “Fmax” to calibrate at approximately1035MHz.

7 Now connect the regulator voltage from the PLL to the VCO. The PLL should now engage and the output frequency is then 1010MHz.

8 If everything has gone right so far, measure the regulator voltage on the VCO again and use “Fmin” to select approximately 3.8 to 4.0V.

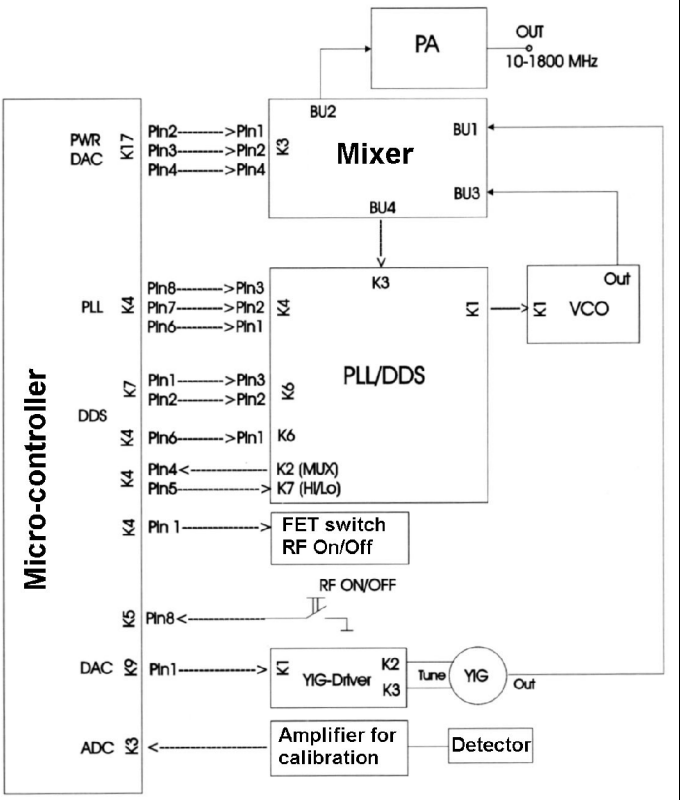

Fig 36: Diagram showing the interconnections between the various assemblies.

Finally, the calibration function (PWR) must be carried out for the power, and immediately afterwards the fully automated calibration function (FRQ) can be carried out for the digital frequency response correction. Both functions are described in greater detail below.

Help

- Should the PLL not engage in the range between 10 and approximately 100MHz, check whether the Hi/Lo switching for the PLL reference frequency is functioning correctly.
- Should the PLL not engage at the top end of the band, check the regulator voltage. Re-balance if necessary, using “Fmax”. (3.8 – 4.0V)
- Should the PLL not engage at 10MHz, check the regulator voltage on the VCO. Increase it to 4.0 to 4.2V if necessary.

Frequency calibration

After a warm up period of approximately 15 minutes, the output frequency can be set, using the R5 trimmer, at the TXCO, with the help of a precise frequency counter. A fine adjustment can also be carried out later using software.

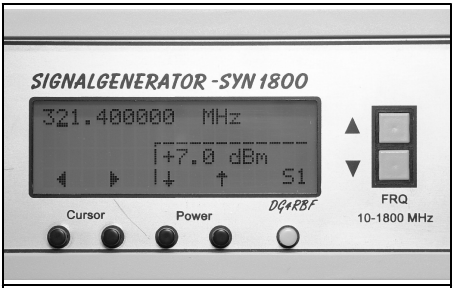

Fig 37: Display showing the five operating buttons.

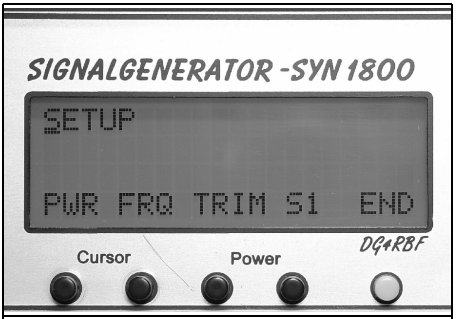

Fig 38: Display showing setup menu.

6.

Operation and functions of software

The display used has 4 lines, so that the lowest line can be used for annotating buttons positioned beneath it.

Fig 37 shows the display with the 5 operating buttons below the display and the two separate buttons near the display.

The first two buttons below the display can be used to move the cursor (in the diagram is under the 2) right or left. The frequency buttons (near the display) can then be used to change the corresponding position of the frequency. Since the frequency setting is programmed with an overrun, the frequency can be adjusted simply and quickly.

The next two buttons below the display are used to adjust the output in 0.1dB steps. Here a progressive adjustment speed has been used, which again makes it easier to operate. The fifth button (S1) has two functions: a short press means the high/low switching for the PLL is manually altered. If this button is pressed for approximately 3 seconds the display will change to the setup menu, which can be seen in Fig 38.

Setup functions

- PWR = power calibration (and balancing of R34)
- FRQ = fully automatic frequency calibration
- TRIM = fine trim for precision of frequency
- S1 = switchover parameters for S1 /High/Low switching of PLL
- END = end of setup menu

6.1 Power calibration

Before the calibration routines are carried out, the equipment should be allowed to warm up for about 15 minutes.

Set the frequency to 100MHz and activate the button [PWR] in the setup menu. The message: CAL Min (R34) appears. Now you must connect an mW meter to the output of the signal generator, using R34 on the mixer board set the minimum level (approximately -10dBm to -5dBm). Then activate the button [SET].

Now the power is calibrated in 1dB steps between +13dBm and 0dBm, with the mW meter remaining connected for this purpose.

Now the message: CAL +13dBm XXXX appears

Fig 39: Display for automatic frequency calibration.

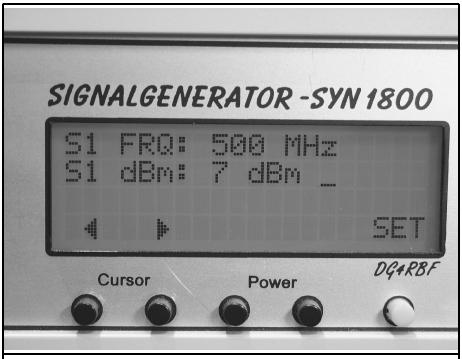

Fig 40: Display showing High/Low switching parameters.

Using the cursor button [< >], set the power to +13dBm. The 4 digit number, which is displayed behind +13dBm, should lie somewhere between 3000 and 3500. Should the value lie outside this range, the voltage divider after the DA converter (LTC1257) should be adjusted. If +13dBm is selected, this is confirmed with the button [SET]. Next,: CAL +12dBm XXXX appears. Set the power level to the pre-set power of +12dBm, once again using the cursor button [< >], and confirm using [SET]. Repeat this procedure down to 0dBm.

6.2 Fully automatic frequency calibration

Immediately after carrying out the power calibration for +13dBm to 0dBm, you should carry out the fully automatic frequency calibration. Connect up a good diode detector to the output of the signal generator and connect the DC voltage output of the detector to the input of the DC amplifier (OPV) on the rear panel of the equipment. When the button [FRQ] is activated in the setup menu, the display shown in Fig 39 appears. The four-digit number that is displayed in the second line is the value for the AD converter. Set the OPV amplification so that a value between 3900 and 4000 is displayed. If the [START] button is pressed, the fully automatic frequency response calibration is started. You can follow the process on the display. The complete procedure lasts approximately 25 minutes. Some more detailed information on the significance of the values displayed during the calibration procedure:

- 1st line: shows the theoretical value for the ADC at the corresponding power level
- 2nd line: shows the instantaneous frequency
- 3rd line: shows the actual value for the ADC
- 4th line: shows the difference detected, which is saved in the EEPROM as a correction value.

The process is terminated automatically and the system returns to normal mode. Every time this routine is carried out, the pre-setting for the high/low PLL switching is subsequently set to +8dBm.

6.3 Trim - fine trim for precision of frequency

This function can be used to fine trim the output frequency. The value is set using the cursor button and confirmed with [SET].

6.4 Switching parameter for high/low switching of PLL

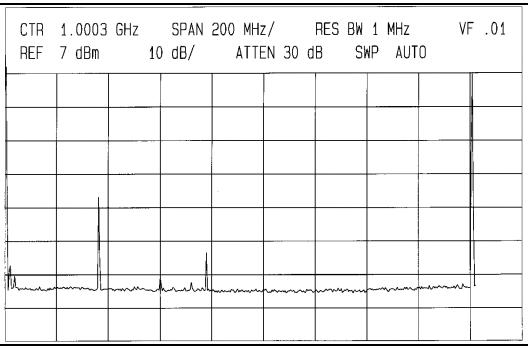

Fig 41: Output signal plot of the 10 - 1800MHz synthesised signal generator.

The parameters for the high/low switching of the PLL can be selected here if necessary The switching frequency can be selected first, using the cursor button, and confirmed using [SET]. Next the second line shows the power reading at which switching should take place. This can be selected in the same way. See Fig 40.

6.5 End of setup menu

Pressing the button [END] will end the setup menu.

6.6 Digital Level ON/OFF

If the fifth button (S1) is pressed and held down, the digital power correction can be switched on and off alternately.

6.7 Reset function

If the first cursor button is pressed and held down, the default parameters will return. But the calibration data in the EEPROM are not deleted.

6.8 Signal plots

Figs 41 an 42 show harmonics and signal quality at various frequencies from 100MHz to 1800MHz.. The plots were carried out using an HP8569A spectrum analyser.

6.9 Boards

If there is sufficient demand, the author will have some boards manufactured professionally. Individual YIG oscillators and VCO's are also still available. Enquiries by E-Mail please to: Info@DG4RBF.de

Any modifications or improvements can be found on the author's homepage. www.DG4RBF.de

The author has been using the signal generator for approximately 1 year and it works perfectly.

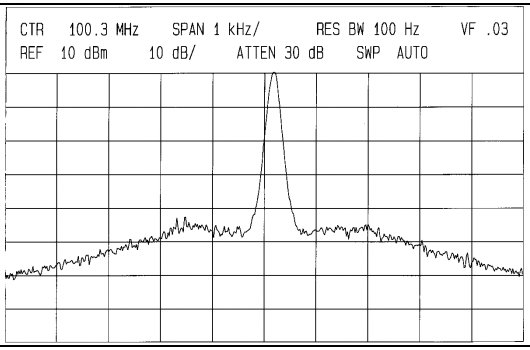

Fig 42: Output signal plot of the 10 - 1800MHz synthesised signal generator.

Table 2: Parts list for micro-controller.

IC1	24C64
IC2	LTC1286
IC3	AT89C55
IC4	7805
IC5	LTC1257
R1	5KΩ
R2,7,8	10Ω
R3	10KΩ
R4	1KΩ
R5	8 x 10KΩ
R6	100Ω
R12,13	10Ω
C1	3.3µF
C2,9,13	100nF
C3,4	27pF
C5,7,8	10µF
C6	2.2nF
C10,11	10µF
C12	0.1µF
C14	10µF
K1	K1 x 16
K2,3,7,9	K1 x 2
K4,5	K1 x 8
K6,22	K1 x 3
K8	K1 x 5
K12,18,23	K1 x 2
K16,20	K2 x 5
K17,21	K1 x 4
LCD1	LCD20 x 4
Q1	18.432MHz
SW-11	Conrad #705115

4 x black caps Conrad ~705115
1 x Yellow cap Conrad # 705078

Table 3: Parts list for VCO.

IC1	78L09
T1	BFP420
VC01	VCO
R1	390Ω
R2	22KΩ
R3	1.5KΩ
R4	22Ω
C1	100pF
C2	2.2pF
C3,5	5pF Sky
C6,8	10µF
C7	1µF
C9,12	1nF
C10	5pF
C11	2.7pF
L1	0.1µH
K1,2	K1 x 1
BU1	SMA with cable or semi ridgid

Table 4: PA parts list.

IC1	GAL-6
R1	47Ω
R2	39Ω
C1,2,3	1nF
C4	1µF
BU1,2	SMA
K1	K1 x 1

Table 5: PLL/DDS parts list.

IC1	ADF4112
IC2,5,6	78L05
IC3	TL431 (2.5v)
IC4	AD9850
IC7,8,9	MSA886
T1	BF324
T2	IRF9520
T3	2N7000
R1,19	4.7K
R2,14,25,26	51
R3	3.3K
R4,9,10,29	1K
R5	680
R6	220K trimer
R7,12,13	22K
R8	470K
R11	24

R15	150
R16,17,18	100K
R20	1.5K
R21	6.8K
R22	470
R23,24	150
R27	47K
R28	100K
R30	22
C1	100pF
C2,30,31	1nF
C3	6.8nF
C4	0.047F
C5	56pF
C6	100pF
C7,24,34,35	4.7nF
C8,9,36,37	10F
C10,11,12	2.2nF
C13,14,15	10F
C16	22nF
C17,20	270pF
C18,19	560pF
C21,22,23,32,33	10nF
C25	4.7pF
C26	2.2pF
C27,28	45pF trimer
C29	10pF
C38	1F
C39	100nF
L1,2,3	1H
L4	10H
L5,6	0.47H
TCX01	TCXO 13.00MHz
D1	LED
F1	SFE10.7MA
K1,2,3	K1 x 1
K4,5,7	K1 x 4
K6	K1 x 3

Table 6: YIG parts list.

IC1	TL431 (2.5v)
IC2	OP27J
Y1	BDX54B
T2	2N7000
D1	IN4148
R1,9,12	1K
R2,11	10K
R3,4	22K
R5	4.7K
R6	47K
R7	3.9K
R8	15
R10	2 (see text)
C1	10nF
C2,3	1.5F
C4	0.22F
C5	100F
C6	470F 6.3v
C7	100nF
C8	0.1F
C9,10	1F
C11	10F
K1-6	K1 x 1
OSC1	YIG 2-4GHz

7.0

Parts lists

Tables 2 - 6 show the parts lists for the main assemblies

8.0

Literature references

[1] Author's homepage:
www.DG4RBF.de

[2] Author's E-mail address:
Info@DG4RBF.de

[3] Analog Devices data sheet
www.analog.com